CLAIMS

What is claimed is:

1. Latch circuitry for high frequency operations, comprising:

a latch coupled to receive a differential input, the latch producing a latched output;

first buffer coupled to receive the latched output, the first buffer producing a first buffered output;

second and third buffers coupled to receive the first buffered output wherein the second buffer produces a second buffered output for a first operation and wherein the third buffer produces a third buffered output for a second operation; and

peaked load circuitry coupled to at least one of the latch, the first, second and third buffers for producing a peaked response at a specified frequency of operation, the peaked load circuitry for increasing impedance and a corresponding voltage level at the specified frequency to at least one of the latch, first and third buffers, respectively.

2. The latch circuitry of claim 1 wherein peaked load circuitry includes a peaked load module that is coupled to each of the latch, the first and third buffers.

3. The latch circuitry of claim 2 wherein each peaked load module comprises a resistive element coupled across a gate and one of a source or drain of a field effect transistor.

4. The latch circuitry of claim 3 wherein each peaked load module comprises a resistive element coupled across a gate and a drain of a n-type MOSFET.

5. The latch circuitry of claim 4 wherein the resistive element further comprises a selectable resistive load coupled to logic for setting a desired frequency of operation for an increased output signal magnitude.

6. The latch circuitry of claim 3 wherein each peaked load module comprises a MOSFET configured capacitor and further wherein a selectable capacitive load is coupled to logic for setting a desired frequency of operation for the increased output signal magnitude and is further coupled in parallel with the MOSFET configured capacitor of the peaked load module.

7. The latch circuitry of claim 1 wherein the peaked load circuitry is coupled to the latch and to the first and third buffers only.

8. The latch circuitry of claim 1 wherein the second buffer isolates the first operation from the second operation by discharging a kickback signal produced by the first operation.

9. Latch circuitry for high frequency operations, comprising:

input stage coupled to receive an input signal and a clock signal as a bias signal, the input stage producing a current that is proportional to an input signal magnitude while biased by the clock signal;

peaked load stage coupled to the input stage wherein the peaked load stage produces an output voltage based upon the current produced by the input stage and further based upon a frequency of current produced by the input stage;

latching stage coupled to receive a complementary clock signal as the bias signal and coupled to the input stage and to the peaked load stage, the latching stage for maintaining

the output voltage while biased by the complementary clock signal.

10. The latch circuitry of claim 9 wherein the input stage comprises a differential pair of MOSFETs having commonly coupled sources that are further coupled to an input stage biasing MOSFET.

11. The latch circuitry of claim 10 wherein the input stage biasing MOSFET is further coupled to an input stage biasing resistor.

12. The latch circuitry of claim 10 wherein the input stage produces a differential input current.

13. The latch circuitry of claim 12 wherein the peaked load stage comprises a pair of peaked load modules wherein each peaked load module of the pair of peaked load modules is coupled to receive the differential current produced by the input stage and produces a differential output voltage based on the differential input current.

14. The latch circuitry of claim 13 wherein each peaked load module of the pair of peaked load modules comprises a MOSFET and a resistive element coupled across a gate and a source of the MOSFET.

15. The latch circuitry of claim 14 wherein each peaked load module of the pair of peaked load modules comprises at least one selectable capacitor coupled across a gate and a drain of the MOSFET.

16. The latch circuitry of claim 15 wherein each peaked load module of the pair of peaked load modules comprises at least one selectable resistor coupled across a gate and a drain of the MOSFET.

17. The latch circuitry of claim 15 wherein the latching stage is coupled to receive the differential output voltage wherein the latching stage maintains the differential output voltage while biased by the complementary clock signal.

18. The latch circuitry of claim 17 wherein the latching stage comprises a differential pair of MOSFETs having commonly coupled sources that are further coupled to a latching stage biasing MOSFET.

19. The latch circuitry of claim 18 wherein:

a first MOSFET drain is coupled to a first peaked load module and a first MOSFET gate is coupled to a second peaked load module; and

a second MOSFET drain is coupled to the second peaked load module and a second MOSFET gate is coupled to the first peaked load module.

20. Buffer circuitry for high frequency operations, comprising:

input stage coupled to receive an input signal and a bias signal, the input stage producing a current that is proportional to an input signal magnitude while biased by the clock signal; and

peaked load stage coupled to the input stage wherein the peaked load stage produces an output voltage based upon the current produced by the input stage and further based upon a frequency of current produced by the input stage.

21. The buffer circuitry of claim 20 wherein the input stage comprises a differential pair of MOSFETs having commonly coupled sources that are further coupled to a drain of an input stage biasing MOSFET.

22. The buffer circuitry of claim 21 wherein a source of the input stage biasing MOSFET is further coupled to an input stage biasing resistor further coupled to a negative supply.

23. The buffer circuitry of claim 21 wherein the input stage produces a differential input current.

24. The buffer circuitry of claim 23 wherein the peaked load stage comprises a pair of peaked load modules wherein each peaked load module of the pair of peaked load modules is coupled to receive the differential current produced by the input stage and produces a differential output voltage based on the differential input current.

25. The buffer circuitry of claim 24 wherein each peaked load module of the pair of peaked load modules comprises a MOSFET and a resistive element coupled across a gate and a source of the MOSFET.

26. The buffer circuitry of claim 25 wherein each peaked load module of the pair of peaked load modules comprises at least one selectable capacitor coupled across a gate and a drain of the MOSFET.

27. The buffer circuitry of claim 26 wherein each peaked load module of the pair of peaked load modules comprises at least one selectable resistor coupled across a gate and a drain of the MOSFET.

28. A method for producing a peaking function for high data rate input signals, comprising:

receiving a differential input signal from an input stage;

coupling the received differential input signal to a peaked load stage comprising a MOSFET configured capacitor, a

resistive element, a selectable capacitor, a selectable resistor, and an N-type MOSFET;

producing a peak in the differential input signal at a desired frequency of operation, which peak is a function of the selectable resistor and the selectable capacitor; and

coupling the peaked differential input signal from the peaked load stage to an output as a peaked differential output signal.

29. The method of claim 28 wherein the selectable resistor comprises one of a linear region MOSFET and a discrete resistive element.

30. The method of claim 28 wherein the selectable capacitor comprises one of a MOSFET configured capacitor and a discrete capacitive element.